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U. S. Navy Underwater Sound Laboratory
Fort Trumbull, New London, Connecticut

ECAP: A DESIGN REVIEW TOOL.

by

Alfred A. Filippini

USL Technical Memorandum No. 2134.4-597-67

INTRODUCTION

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This memorandum is written to: inform Laboratory personnel that ECAP, a general purpose electronic circuit analysis program, is available for their use; describe this program; and provide instructions concerning its use. Section I is a general explanation of the function of the program, Section II contains a description of the software with which the ECAP user must be familiar, and the step-by-step computing procedure is detailed in Section III. Wherever possible in Section III, examples rather than lengthy discussions are used to demonstrate proper procedure.

No attempt has been made to duplicate completely the information in the ECAP Operators Manuals references (a), (b), and (c). Instead, an attempt has been made to present sufficient information to permit the reader to program circuit analyses after reading this document. When specific problems arise, however, the Operators Manuals should be consulted.

# SECTION I: PROGRAM DESCRIPTION

The Electronic Circuit Analysis Program (ECAP) is a general purpose program which allows USL engineers to utilize the computer facilities at the Laboratory to analyze electronic circuits. The International Business Machines Corporation and the Norden Division of United Aircraft Corporation jointly developed ECAP, and TRW Systems converted it for use on USL's IBM 704 computer.

ECAP is really a combination of three analysis programs:

- (1) a DC Analysis Program,
- (2) an AC Analysis Program, and
- (3) a Transient Analysis Program

Approved for public release;
Distribution Unlimited

For the DC Analysis Program the circuit must be described using Burl (/) to USE/USE 254200

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resistors, independent voltage sources, dependent current sources, and independent current sources. The computer will calculate and print out all the voltages and currents, power dissipation, worst case voltages, sensitivities, and standard deviations if so directed by program control cards. In addition, certain intermediate results such as current, impedance, and admittance matrices will be printed out if requested by the engineer. The circuit parameters may be modified, permitting the engineer to study the effects of component variations on circuit performance.

Only resistors, capacitors, inductors (including mutual inductors), independent voltage sources, independent current sources, and dependent current sources can be used to describe a circuit for an AC analysis. This program will compute and print out at a single frequency all voltages, currents, element power dissipations, current matrices and admittance matrices if so desired. As with the DC Analysis Program the circuit parameters (including frequency) may be varied.

The Transient Analysis Program requires that the circuit be modeled with resistors, capacitors, inductors; DC independent and time-varying independent voltage sources; DC independent, time-varying independent and dependent current sources; and logical switches. Circuit parameters can be automatically altered when branch currents reverse direction through the use of the Logical Switch. With the Transient Analysis Program all node voltages and element currents are printed out as a function of time.

ECAP is a very useful design review tool. The DC Analysis Program can be used to evaluate DC bias currents and voltage; determine stress ratios; perform worst case, statistical, or sensitivity analysis of circuits. A frequency analysis can be conducted by use of the AC Analysis Program to obtain open-loop frequency response data. With the Transient Analysis Program and piece-wise linear models of non-linear devices, actual circuit performance as a function of time can be duplicated. As a result, biasing of circuits involving non-linear devices can be studied, the step response of a circuit can be analyzed, rise and fall times can be measured and the output of a non-linear circuit for various combinations of inputs can be computed using the Transient Analysis Program.

## SECTION II: PROGRAMMING SOFTWARE

The USN/USL ECAP user must familiarize himself with only two printed forms. They are the Compilation/ Check-Out/ Production Request and the Fortran Coding Form and Data sheet. Both are available in the USL Computing Center.

The Compilation/ Check-Out/ Production Requests properly completed for each type of analysis, are shown in figures 1, 2, and 3. Because the request form is returned to the ECAP user following the execution of each analysis, the request is filled-in only once for each type of analysis. The information for items 1, 2, 4, and 5 is unique to each ECAP User; the other items on the form need not be altered.

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Figure 4 is a Fortran Coding Form and Data Sheet. The information in the heading is self-explanatory and the body of the form is used to describe the punched cards required by the ECAP user.

The punched cards necessary to utilize ECAP are grouped into six categories:

- (1) Time Cards,
- (2) Comment Cards,
- (3) Command Cards,
- (4) Data Cards,
- (5) Solution Control Cards, and
- (6) Output Specification Cards.

Computer Center Personnel punch the Time Card (see figure 5) from the Compilation/ Check-Out/ Production Request. When submitted with the program deck, it will be retained by the Computer Operator.

Comment Cards are characterized by a C in column 1 and a message in the data field which extends from column 7 to column 72. These cards serve no useful programming function; the message is simply reproduced on the output data sheet. Cards with only a C in column 1 cause line spaces in the print-out.

Each analysis program deck should begin with Comment Cards which identify the output data. The format for these Identification Cards has been established by the author and has proved useful to the author and computer center personnel.

Three identification cards are used:

- (1) A Program Description Card,
- (2) A Circuit Description Card, and
- (3) A Date Card.

The information for these cards is demonstrated in figure 6. The first card identifies the program, the computer, the program user, his code, and his extension. The circuit Description Card identifies the circuit being analyzed and the third card identifies the run number, and date.

There are five cards in the Category Command Cards. They are:

- (1) AC Analysis,
- (2) DC Analysis,
- (3) Transient Analysis,
- (4) Execute, and
- (5) Modify Cards.

The data for these cards is shown if figure 7. Only one Analysis

Card is used per program deck. Modify cards may only be used with the AC and DC Analysis Programs. An Execute Card is paired with the Analysis Card and every Modify Card.

There are five types of Data Cards:

- (1) B-Cards,
- (2) T-Cards,
- (3) M-Cards,
- (4) S-Cards, and
- (5) Source Cards.

The Standard Branch written into ECAP is shown in figure 8. The directions of positive currents and the polarities of positive voltages are shown on the figure. Reversed directions and polarities must be indicated by negative values on the Data Cards.

The B-Card is used to describe the initial and final nodes, the linear element, the time-invarient independent voltage source, the time-invarient independent current source, and initial conditions. Figure 9 demonstrates the relationship between the B-Card and the Standard Branch.

The Branch number is written in columns 1 through 5 of the data card and the remainder of the data must appear in columns 7 through 72. The node numbers are put on the data card in sequence, the initial node first. Therefore, the directions of positive currents and the polarities of positive voltages are established by the users selection of the initial node. Ground nodes are assigned the number 0. Following the node numbers the parameter values appear separated by commas. Initial conditions (i.e., voltage across capacitors and currents through inductors at the initial time of a Transient Analysis) are established by EO and IO statements. Note that any Fortran coding of numbers is acceptable to describe parameter values. For those not familiar with the coding of scientific notation, 1.2 x 10 is written in Fortran 1.2 E3.

The T-Card describes the dependent current source in each branch. Like the B-Card, Columns 1 through 5 are used only for the number of the dependent source. The control and source branch numbers, in that order, and the current gain which relates the element current of the control branch to the source current appear in the data field. Examples of the use of the T-Card may be found in figure 10.

The mutual inductance between two branches containing inductors is described by the M-Card. The format of this card is similiar to that of the T-Card. However, the order of the branch numbers is unimportant. The application of M-Cards is demonstrated in figure 11.

The logical switch operation is controlled by the S-Card. Like the other cards discussed so far, the S-Card number is put in columns

1 through 5. The element current of a branch is sensed and when that current is zero or negative, the switch is off; when the current is positive, the switch is on. As the state of the switch changes, the values of circuit parameters may be changed. Look at the Fortran statement for the S-Card in figure 12. The S-Card causes the element current of branch 2 to be sensed. When the current changes, branches 2, 3, and 4 will be affected. Initially the state of the switch is off (i.e., the current in branch 2 is zero or negative). With Sl in the off state, the resistance of branch 2 is 500, the capacitance of branch 3 is 2 of, and the beta of the dependent current source is 100. When S1 goes on (i.e., branch 2 current goes positive), the resistance of branch 2 goes to 550A, the capacitance of branch 3 goes to 3uf, and the beta of Tl goes to 125. Note that the beta of Tl is altered by having the switch action affect branch 4 (the control branch), not branch 1 (the source branch). Should the current return to zero or go negative, the parameters would return to their initial values.

To describe time-varying independent voltage and current sources, three types of Source Cards are used:

- (1) Non-Periodic,
- (2) Periodic, and
- (3) Sinusoidal.

The Non-Periodic Source Card data is shown on line 2 of figure 13. Columns 1 through 5 of the card define the type of source (current or voltage) and the number of the branch in which it is positioned. In the data field, the number of time steps between changes in source values appears in parentheses, and the voltages or currents at each increment of time beginning at start time appear separated by commas. The Time Step on line 3 indicates the interval at which circuit performance is computed. A linear change in amplitude between time increments is assumed and the value of the final entry is maintained until final time is reached. The number of voltage entries is limited to 126.

Figure 14 demonstrates a Periodic Source Card. Except for the addition of a P in the data field to designate a periodic function, the data entries are identical to those of the Non-Periodic Source Card. The first and last value of voltage or current should be equal because the function is periodic. As for the Non-Periodic source the maximum number of entries is 126.

A Sinusoidal Source Card is described in figure 15. Columns 1 through 5 are used to describe the type of source and branch number as with the Non-Periodic and Periodic Source Cards. In the data field, however, SIN is used to indicate that a sinusoidal source is desired and the period in seconds is put in parentheses. The peak value, the DC average value, and the initial time shift follow, separated by commas.

For an AC Analysis, B-Cards, T-Cards, and M-Cards; for a DC Analysis, only B-Cards and T-Cards; and for a Transient Analysis, B-Cards, T-Cards, S-Cards, and Source Cards are used.

Continuation Cards may be used if the data is in excess of the data field of one card. A Continuation Card is characterized by an asteric in column 6. The data field of the Continuation Card can then be considered an extension of the previous Data Card.

The number of Data Cards is limited to:

200 B-Cards (limited to 50 inductors if M-Cards are used) 200 T-Cards, and

200 S-Cards.

In addition, the circuit must contain no more than 50 nodes.

The data cards used with Modify-Execute Card pairs have a modified format. First, the data field of the card need only describe the parameter to be changed. Second, multiple variations of a parameter may be written into one statement which defines the initial value, the number of steps (in parentheses), and the final value. Examples of these Data Cards can be found in figure 16. No more than 50 parameter changes in one parameter modification are allowed.

Solution Control cards are unique to the type of Analysis being performed. Figures 17, 18, and 19 lists the Fortran statements for Solution Control Cards.

If the AC Analysis Program is being used there is only one Solution Control Card and this card must appear in the program card deck to specify frequency. When the Frequency Card is used to control the initial computation, only one value of frequency may be specified. When the Frequency Card is used with a Modify-Execute Card Pair, a single value, and arithemetic progression, or a geometric progression may be specified. See figure 17. For an arithmetic progression the initial value, the number of evenly spaced steps, and the final value are written. The number of steps must appear in parentheses with a plus sign. For a geometric progression, the ratio is specified in parentheses instead of the number of steps. The lack of a plus sign indicates a geometric progression.

Three Solution Control Cards may be used if a DC Analysis Program is in use. If the Sensitivity Card appears in the card deck, the partials and sensitivities of each node voltage with respect to each resistance, beta, and source value is computed and printed out. If the Worst Case Card appears in the deck, the worst case minimum, worst case maximum, and nominal node voltages for each node specified

on the Worst Case Card are printed out. If no node numbers are written all node voltages will be printed out. For this computation the minimum and maximum values or the tolerances, in addition to the nominal parameter values, must be specified. See figures 9 and 10 for examples of how to specify the extremal values. The Standard Deviation Card causes the standard deviation of each node voltage to be printed out. For this computation, the  $\frac{+}{3}$  standard deviation values of the circuit parameters are specified with the same format that the minimum and maximum values are specified for a Worst Case Analysis.

When the Transient Analysis is being run, ten Solution Control Cards may be used. See figure 19. The Time Step Card must appear in every transient analysis. However, if any of the other 9 cards are omitted, the values listed in figure 20 are assumed. The Output Interval Card specifies the number of Time Steps between data printouts. When the Equilibrium Card is entered in the card deck, a solution is obtained with the inductors in the circuit replaced by short circuits and capacitors by open circuits. The values of open and short circuits are specified with the appropriate Solution Control Cards. The 1-ERROR, 2-ERROR, and 3-ERROR Cards control the acceptable magnitude of the sum of the nodal current unbalances, the accuracy of the switch accutation time printed out, and the value of the time steps immediately after an initial condition solution. Reference (a) should be consulted if it is desired to use these ERROR cards.

The Output Specification Cards allow control by the ECAP User of the data printed out. See figure 21.

For the AC and DC Analysis Programs:

- (1) node voltages (NV) (VOLTAGES),
- (2) element voltages (CV),
- (3) branch voltages (BV),(4) element currents (CA),
- (5) branch currents (BA),
- (6) element power dissipation (BP), and
- (7) miscellaneous outputs (MI) (MISCELLANEOUS)

can be printed out. The various voltages and currents are designated on the diagram of the Standard Branch (figure 8). Element power is the product of element voltage and element current. Miscellaneous outputs are current and impedance matrices for AC Analyses; and admittance, current, and impedance matrices for DC Analyses.

For the Transient Analysis Program, the only data permitted to be printed out is:

- (1) node voltages (NV) (VOLTAGES) and
- (2) element currents (CA) (CURRENTS).

## SECTION III: COMPUTING PROCEDURE

The author recommends the computing procedure established in this section of the memorandum. Although other procedures will work as well, the author has demonstrated that delays and errors are minimized by following the steps outlined here.

To demonstrate the suggested computing procedure, the bias, frequency response, and response to a square wave of the circuit diagramed in figure 22 will be determined. The DC circuit will be subjected to a Transient Analysis to determine bias conditions; the worst case bias conditions will be determined using the DC Analysis Program once the nominal bias conditions have been established; the frequency analysis will be performed on the circuit with the AC Analysis Program; and finally, the Transient Analysis Program will be used to determine the step response of the circuit.

Figure 23 is the ECAP DC Circuit Diagram. This diagram is drawn directly from the Standard Circuit Diagram (figure 22) and differs very little from a standard dc equivalent circuit. Note, however, that care has been taken to arrange the circuit elements such that a Standard Branch (figure 8) appears between every pair of nodes, to indicate the direction of element currents, and to number the nodes and branches using consecutive numbers. Ground nodes are numbered 0.

Models for non-linear devices should be carefully selected. There is no one model which meets all applications. This is especially true of transient models. The author urges each ECAP user to select a model which duplicates with sufficient accuracy the parameters which have the greatest effect on the particular outputs desired. The models in figures 24 and 25 were carefully chosen to be only as sophisticated as they need be. Because they duplicate the VBE-IB and VCE-IC characteristics of the 2N930 type transistor with sufficient accuracy to determine the bias points, the complex models in figure 24 were selected. However, the simple models diagramed in figure 25 adequately represent the V-I characteristics once the nominal bias points have been determined. The values of the parameters (voltage and resistance) in branches 9 and 11 are based on the results of the analysis using the models in figure 24.

To document the ECAP Data, a Compilation/ Check-Out/ Production Coding Form and Data Sheets must be filled in. Figures 26 and 27 show the Fortran sheets completed for the Transient Analysis of the DC Circuit. Note the difference between the letter Ø and the number 0, the letter I and the number 1.

To expedite the computation, the computer center personnel are assisted by the ECAP user. The completed forms are brought to the

Card Punch Operators' Room where they are date-stamped and left. The ECAP User is called when the cards have been punched and verified. Usually, this takes one day. When the user is called, he returns to the Card Punch Room to receive his original forms plus the punched cards. The cards are then assembled in the proper order:

(1) Time Card

(2) Identification (Comment) Cards,

(3) Analysis (Command) Card,

(4) Data Cards,

(5) Solution Control Cards,(6) Output Specification Card,

(7) Execute (Command) Card,

The cards are then submitted to the Computer Room with the Compilation/Check-Out/Production Request in front of the deck under the elastic band. The Production Log is filled-in as shown in figure 28 and the card deck is put in the "Production" box located in the Computer Center. The output data will usually be available in 4 hours.

The output data for the Transient Analysis of the DC Circuit may be found in Appendix A. The voltages are recorded on the ECAP DC Circuit Diagram in figure 23.

Once the bias points have been determined, the dc transistor models shown in figure 25 result and a Worst Case DC Analysis can be run.

Once again a Request Form (figure 2) and a Coding Form (figure 29) are completed and submitted to the Key Punch Operators, When the punched cards are returned, appropriate cards from the Bias Point Analysis are used to assemble a deck which results in the statements appearing on page B-l of Appendix B. A check should be made to insure that the cards are in the proper order. The extra cards required for data modifications are put in the following order:

(1) Modification (Command) Card,

(2) Data Cards, and

(3) Execute (Command) Card.

The dc output data appears in Appendix B.

Knowing the bias points, the ECAP AC Circuit Diagram (figure 30) and the Transistor Model Diagrams (figure 31) are drawn. An AC Analysis Request Form (figure 1) is completed and the circuit data is transferred to the Coding Forms. Modification of AC Analysis data require that the extra cards be put in the following order:

(1) Modification (Command) Card,

(2) Data Cards,

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(3) Frequency (Solution Control) Card, and

(4) Execute (Command) Card.

The input data statements and the output data appear in Appendix C. The output data is plotted in figure 32.

To determine the response to a step input function, a transient analysis was run. The Transient Circuit Diagram and Transistor Models are shown in figures 33 and 34 respectively. The input step is shown in figure 35. The input and output data are recorded in Appendix D. The output response data is plotted in figure 36. It should be noted that the initial voltage across each capacitor is specified in the input data. In addition, it should be noted that is was necessary to exclude from the transient analysis the 60 microfarad capacitor in the power supply isolation network. Until this was done the accuracy of the current computations at node 5 was inadequate.

#### SUMMARY

This memo was written to introduce the Electronic Circuit Analysis Program to the reader. The author in no way pretends that this memo thoroughly covers the use of ECAP. On the other hand, it is hoped that after reading this memo, most engineers will be able to utilize the available computational tool without reading the IBM ECAP Users Manual (Reference (a) ). However, if and when problems arise, or when additional information is needed, the appropriate reference or references listed in this memo should be consulted.

ECAP is a complex analysis program, especially useful as a design review tool. Breadboarding can be minimized or eliminated with proper use of this program.

Electronic Engineer

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FIGURE 1: AC ANALYSIS REQUEST

USL Tech Memo 2134.4-597-67 CHECK-OUT/PRODUCTION REQUEST HRS. 3ND USNUSL- 3648 (REV. 7/ 66) To Be Called 11. Estimate MIN. (CHECK APPROPRIATE BOXES) B. Production (3) A. Check-Out (2) (COMPLETE ITEMS 1 THRU 11) 2. Tel. Ext. No. 470 3. Coded Job No. 0679 1. Requestor A. FILIPPINI 4. Job Order No. 1-654-00-00 5. Organization Code 2/34.4 6. Open Shop X 7. Fortran 8. Components Used a. Reader c. Mag. Drum S.A.P. L b. Printer d. Punch Closed Shop - - (Fold) SS 6. SS 1. SS 2. SS 3. SS 4. SS 5. 9. Sense Switches used: All assumed up unless checked. Unit In-Out-WRITE TAPE IDENTIFICATION CHECK APPROPRIATE BOXES No. put SYSTEM Save Punch | Plot | Pool List 1 2 ANALYSIS PRØGRAM X DC X INPUT CARDS 4 OUTPUT TAPE X 5 6 7 0 B.C.D. BINARY GAPLESS INPUT TAPE MODE OUTPUT BINARY B. C. D. X Program Stops and Procedures: HPR 5,0 Correct Halt HPR 6,0 = Bad ID Halt NORMAL STOP HPR (0, 1) Special Instructions: BINARY TAPES IN HONEYWELL

8/8/66- 1,000 - FIRST RUN- EXPERIMENTAL

FIGURE 2: DC ANALYSIS REQUEST

USL Tech Memo No 2134.4-597-67 CHECK-OUT PRODUCTION REQUEST To Be Called 11. Estimate MIN. 30 (CHECK APPROPRIATE BOXES) B. Production (3) A. Check-Out (2) (COMPLETE ITEMS 1 THRU 11) 2. Tel. Ext. No. 470 3. Coded Job No. 0680 1. Requestor A. FILIPPINI 4. Job Order No. 1-654-00-00 5. Organization Code 2134.4 6. Open Shop X 7. Fortran 8. Components Used a. Reader c. Mag. Drum S.A.P. Closed Shop b. Printer d. Punch - - (Fold) SS 1. SS 3. SS 5. 9. Sense Switches used: SS 2. SS 4. All assumed up unless checked. 10. Out-Unit In-WRITE TAPE IDENTIFICATION CHECK APPROPRIATE BOXES No. put put SYSTEM Punch Plot Pool List X 2 TRANSIENT ANALYSIS PRØGRAM X INPUT CARDS 3 4 OUTPUT TAPE X 5 6 B.C.D. BINARY GAPLESS INPUT OUTPUT TAPE MODE BINARY B.C.D. Program Stops and Procedures: Correct Halt HPR 6,0 = Bad ID Halt HPR (0,1) NORMAL STOP IN Special Instructions: BINARY TAPES 8/8/66- 1,000 - FIRST RUN- EXPERIMEN TAL

FIGURE 3: TRANSIENT ANALYSIS REQUEST

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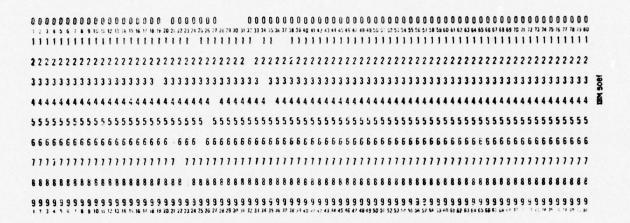
FIGURE 4

345-27-02-11-96

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# FIGURE 5: TIME CARD

L			864			28																			•											F	OR	TR	M :	TA	TE	ME	NT								
1	2		3	4	5	6	7	8	9	10	11	12	1 13	14	1 15	16	17	18	15	20	2	1 2	2 2	3 2	4 2	25 2	6 :	27 2		29 3	0 3	1 3	2 3	3 3	4 35	36	37	31	39	40	41	42	4:	3 4	4 45	46	47	484	19 5	50 :	51
6		T	T	7			E	C	A	P		T	1	E	M		7	0	4		T	A	T	F	1	1	1	1	)		: A	1	1,	T	C		D	E	T	9	3	4	Ι,	4	,		×	П	4	7	0
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FIGURE 6: FORTRAN STATEMENTS FOR IDENTIFICATION CARDS

1			764 M81			8 KT	Γ								. 1604														
1	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	2
1							A	C		A	N	A	L	Y	5	I	S		0	6	7	8							-
	j						D	C		A	N	A	L	Y	S	I	S		0	6	7	9							
	1						T	R	A	N	5	I	E	N	7		A	N	A	1	Y	S	I	S		0	6	8	C
	1						E	X	E	C	U	7	E																
	1						M	4	D	I	F	Y														7			

FIGURE 7: FORTRAN STATEMENTS FOR COMMAND CARDS

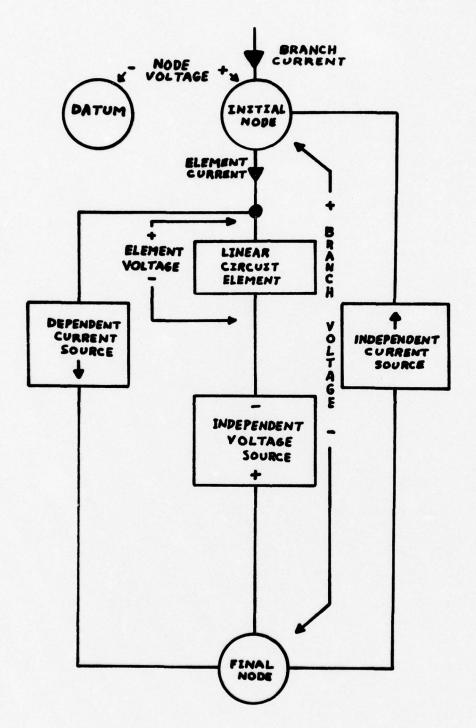


FIGURE 8: THE STANDARD BRANCH

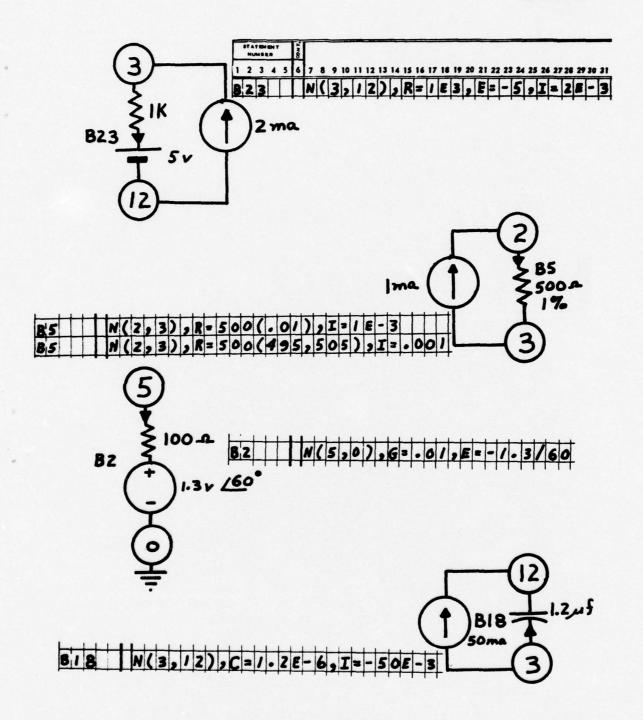
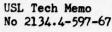


FIGURE 9 : EXAMPLES OF B-CARD DATA



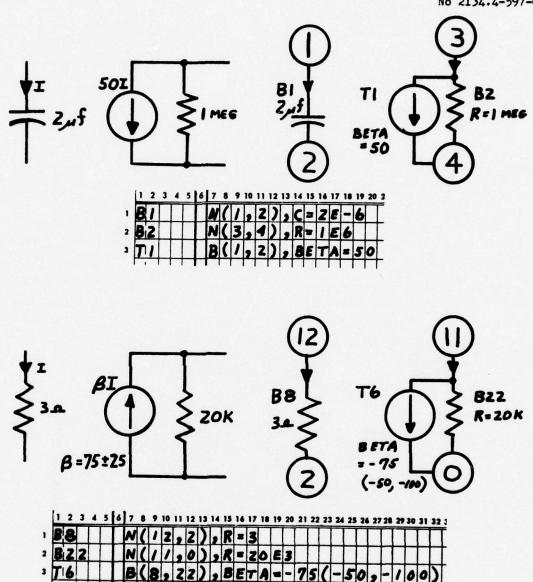
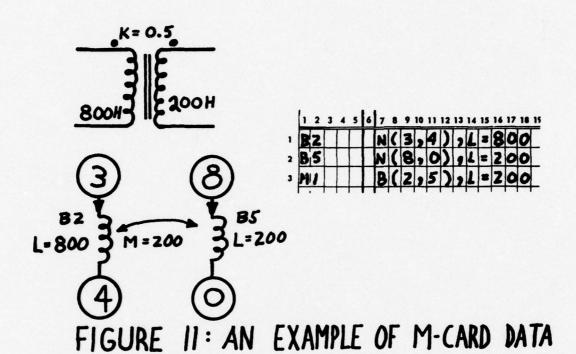
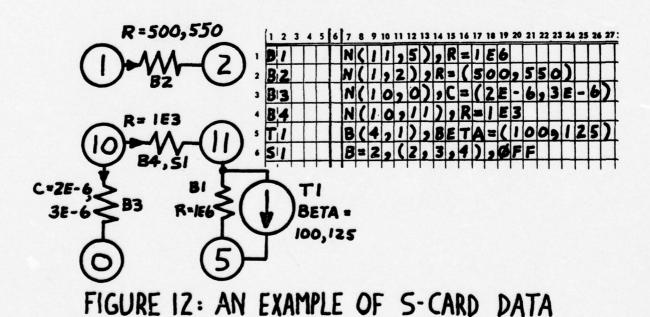


FIGURE 10: EXAMPLES OF T-CARD DATA





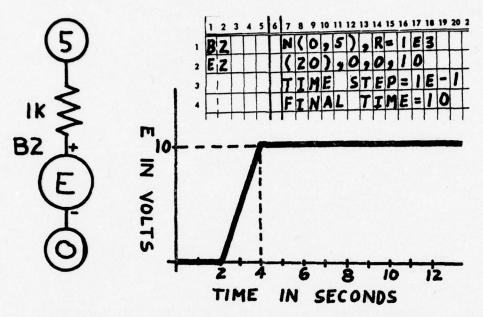


FIGURE 13: AN EXAMPLE OF A NON-PERIODIC SOURCE CARD

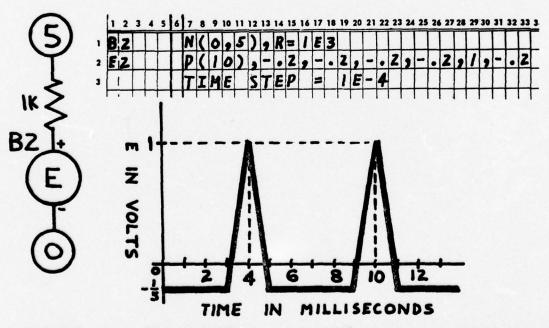


FIGURE 14: AN EXAMPLE OF A PERIODIC SOURCE CARD

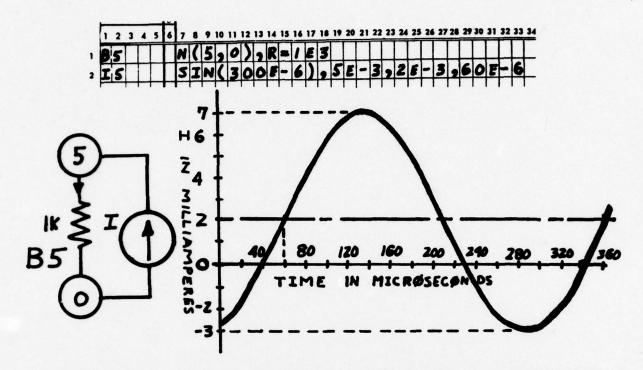


FIGURE 15: AN EXAMPLE OF A SINUSOIDAL SOURCE CARD

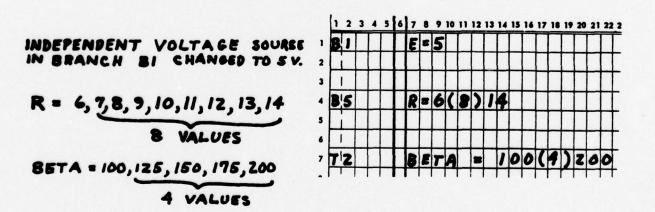


FIGURE 16: DATA FOR USE WITH MODIFY-EXECUTE CARDS

f = 5 KHZ f=5,10,15,20,25 KHZ f=1,2,4,8,...,128,256 MHZ

2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	27
I					F	R	E	0	v	E	N	C	Y		5		5	E	3							H	
1										•										-							
1				-	F	R	E	Q	V	E	N	C	Y		=		5	E	3	(	+	4	<u>)</u>	Z	5	E	3
1							E	•	v	E	4	•	~				1	E	4	7	7	1	2	4	0	F	4

FIGURE 17: AC ANALYSIS SOLUTION CONTROL DATA

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
						5	E	N	S	I	7	I	V	I	T	Y							
						W	6	R	5	T	Ť	C	A	5	E	,	3	,	9	,	1	2	
	1					S	T	A	N	D	A	R	D		D	E	V	Ī	A	Ť	1	٥	N

FIGURE 18: DC ANALYSIS SOLUTION CONTROL DATA

L	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
Γ	T	Г				T	I	M	E		S	T	E	P		=		1	E	-	6			
	i					1	U	T	P	U	7		I	N	7	E	R	V	A	L		=		5
	1					I	N	I	T	I	A	L		T	1	7	E		=		Z	E	•	6
T	1					F	I	N	A	٢		T	I	M	E		=		5	0	0	E	1	3
	1					E	Q	V	I	L	I	8	R	T	V	M								
	1					5	H	6	R	7		3	•	0	0	1								
Γ	T					Ø	P	E	N		=		1	0	0	E	6							
	1					1	E	R	R	Ø	R		=		1	E	-	4						
T	1					2	E	R	R	6	R		=		1	E	-	4						
T	1					3	E	R	R	6	R		=			٥	1							

FIGURE 19: TRANSIENT ANALYSIS SOLUTION CONTROL DATA

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
						Ø	U	T	P	U	T		I	N	T	E	2	Y	A	L		=		1
						I	N	I	T	I	A	L		T	I	M	E		=		0			
						F	I	7	A	L	1	T	I	M	E		=		1	E	1	9		
	!					5	H	6	R	T		=		•	0	1								
Г						0	P	E	N		3		1	0	E	6								
	1					1	E	R	R	ø	R		=			0	0	1						
	1					2	E	R	R	ø	R		=			0	0	1						
						3	E	R	R	6	R		8		1									

FIGURE 20: ASSUMED SOLUTION CONTROL DATA

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	2
						P	R	I	N	T	,	C	U	R	R	E	N	T	5	,	V	ø	L	T	A	6		S
						P	R	I	N	T	,	N	V	,	C	A	,	8	P									
	1					P	R	I	N	7	•	8	V	,	M	I	S	C	E	L	A	N	E	ø	V	5		
	1					P	R	I	N	7	,	N	Y	,	C	V	,	B	Y									
						P	R	I	N	T	,	8	P															
	1					P	8	I	N	T		B	A	•	M	T												

FIGURE 21: OUTPUT SPECIFICATION DATA

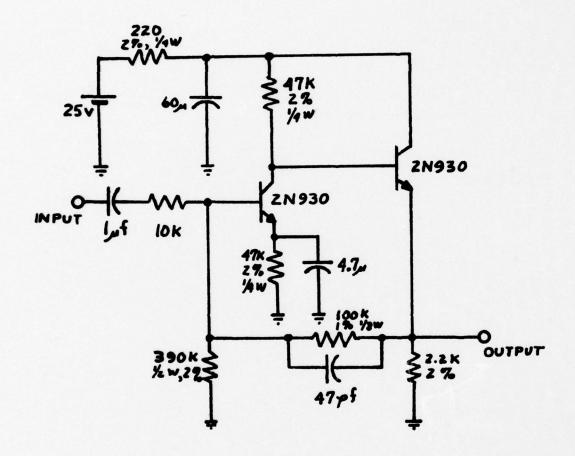


FIGURE 22: STANDARD CIRCUIT DIAGRAM

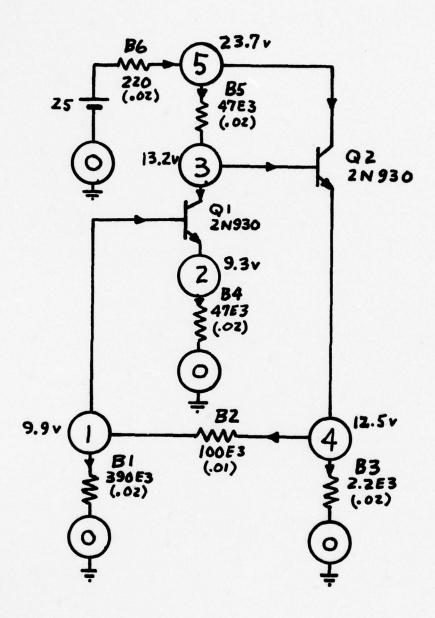
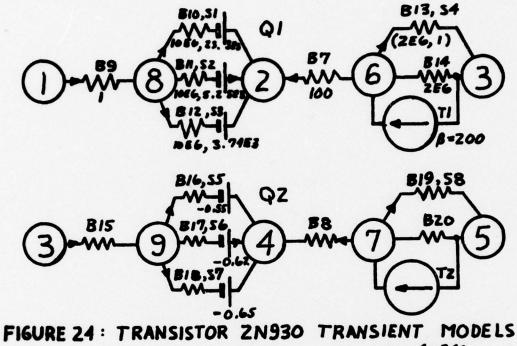
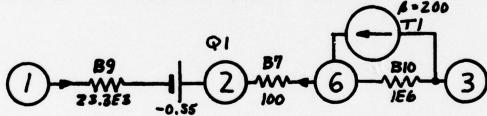


FIGURE 23: ECAP DC DIAGRAM





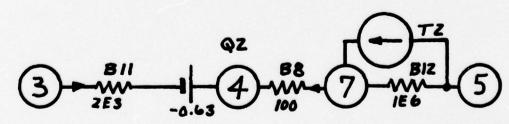


FIGURE 25: TRANSISTOR 2N930 DC MODELS

USL Tech Nemo No 2134.4-507-67 73 74 75 76 77 78 79 80 IDENTIFICATION TR ANSIENT ANALYSIS 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 4 31 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 58 55 58 59 60 61 62 63 64 45 66 67 68 69 70 71 72 THE ECAP JUNE 1966 -654-00-00 6 24 FORTRAN STATEMENT JOB ORDER HO. PAGE ECAP. ISM 704. A FILIPPINE, X470 DEMONSTRATION AMPLIFIER M(8,2),R=(10E6,23.3E3),E=-0.55 B=(0,(0),0),ØFF M(8,2),R=(10E6,5.25E3),E=-0.6E 39-0-=36 0890 B=11,1(11),6FF N(B,2),R=(10E6,3.74E3),E B=12,(12),GFF N(6,2),R=(100 N(6,3),R=(2E6,1) RIAS ANALYSES RUN 1, 30 JUNE 1966 TRANSIENT ANALYSES 0680 THE CIRCUIT ELEMENTS N(190), R=390E3 PROBLEM NC. N(4,0),R=100E3 N(4,0),R=2.2E3 N(2,0),R=47E3 M(5,3), R: 47E3 Ä FORTRAN CODING FORM AND DATA SHEET PREPARED BY ALFRED 470 Q1 , 2N930 1 30025 PHONE EXT. • 1 2 3 4 5 8/0 2 18 2 2 **8** 2 2 8 5 E 1 83 - 81 13 B C 23 23 21 8 12 2

2 2 = • ANALYSIS BIAS : 97 FIGURE

"SL Tech Nemo No 2134.4-597-67 TRANSJENT ----ANALYSIS ECAP TITLE DATE 24 TUNE 1966 1-654-00-00 JOB ORDER NO. FORTRAN STATEMENT PAGE M(3,9), A= 1 M(9,4), A= (1066,23.3E3), E=-0.65 B=16, (16), A=6 M(9,4), A=6 M(9, N(924) 2R= (10E623.74E3) 2E=-0.65 HERARD BY ALFRED A. FILIPPINI 0890 1(5,7),R.266 3(15,20),BETA-200 FINAL TIME = 16-6 B = 135 (13) 2 FF M 33 6 2 A = 266 B (92 14) 28 ETA = 200 TIME STEP = 16-6 (7,5),R=(2E6,1) PROBLEM NO. PRINT, VOL TAGES 7,4), 8= 100 FORTRAN CODING FORM AND DATA SHEET 470 92.3M930 EXECUTE PHONE EXT. 12345 8.17 . 820 25 12 57

=

= • 2 = DATA

ANALYSIS

BIAS

27:

FIGURE

370-90 50-11490

23 75

	REQ	QUESTO	R		OP	ERATOR		
IN by T	Job E.	st. R	equestor	Remarks	Batch 1 BIN 2	nput BCD 3	Prog.	Output Tapo
/30 18			FELIPPINI	ECAP TRANSPOR				
-	+	+						
+	++	+						
+							-	

FIGURE 28: PRODUCTION LOG

USL Tech Nemo No 2134.4-507-67 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 22 24 24 25 24 25 24 25 25 24 25 25 27 26 27 28 27 29 27 29 27 29 27 29 27 24 24 44 45 44 45 44 45 46 47 48 45 51 25 25 25 25 25 25 25 25 25 25 25 26 21 62 24 65 65 65 70 71 72 77 75 77 75 77 70 77 70 70 ---ANALYSES ECAP DC THE 1-654-00-00 DATE 7 JULY 1966 FORTRAN STATEMENT JOS ORDER NO. - 1974 N( (2) 2) 2, R = 1, 2 (2) 2, 2 (2) 3, 4 (2) 3, 2 (2) 3, 4 6630 B(11912) 98ET # 200 WORST CASE91929 3945 PREWTSCORRENTS98P PREPARED BY A. FILTPPINE IN MAN IN CORNOR. PROBLEM NO. (5,7),28-166 FORTRAN CODING FORM AND DATA SHEET 470 8ETA=150 SETA- 150 EXECUTE PHONE EXT. 640

2 = 2 2 2 = 2 2 2 22 2 2 2

2

DATA ANALYSIS 2 : 67 FIGURE

3MD-08 80-1149

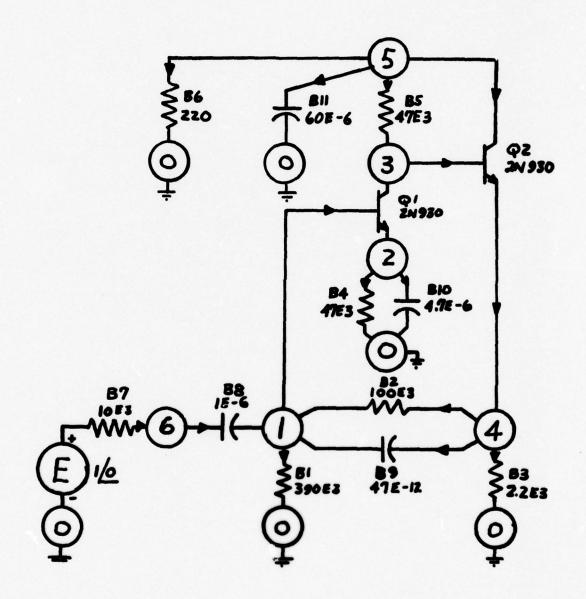


FIGURE 30: ECAP AC CIRCUIT DIAGRAM

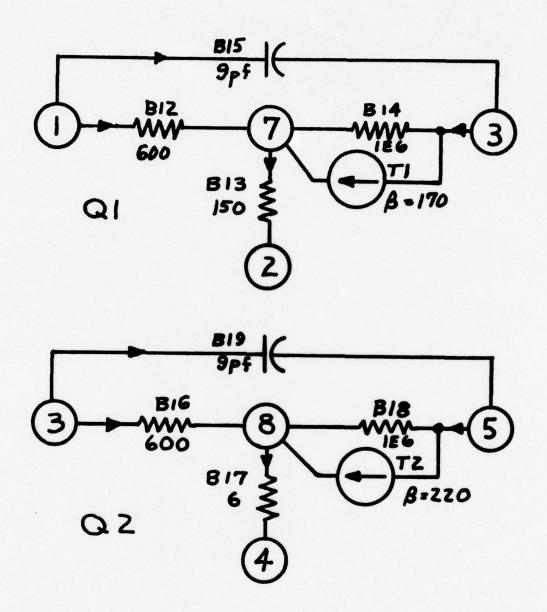
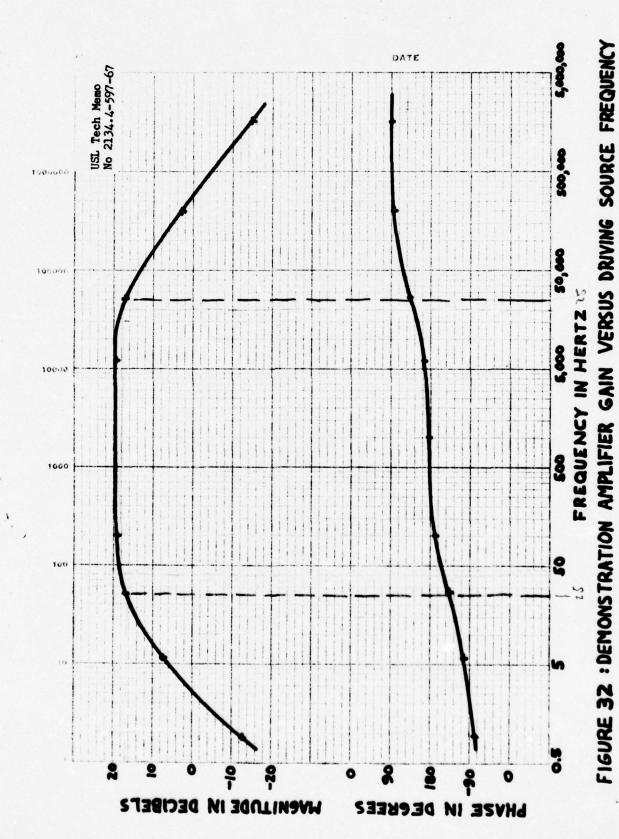


FIGURE 31: TRANSISTOR 2N930 AC MODELS



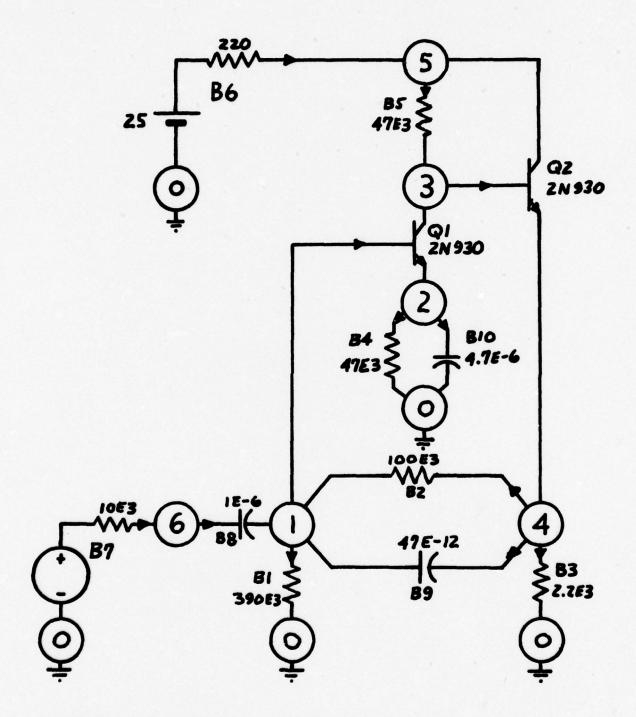


FIGURE 33: ECAP TRANSIENT DIAGRAM

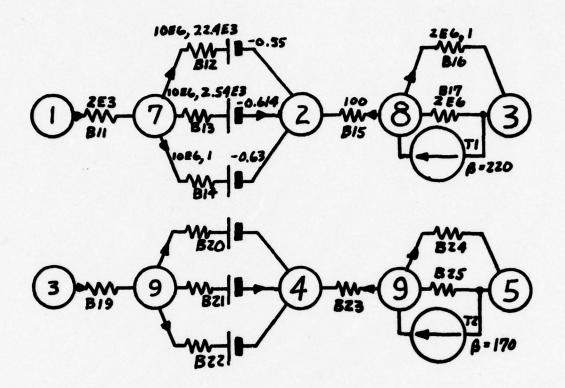
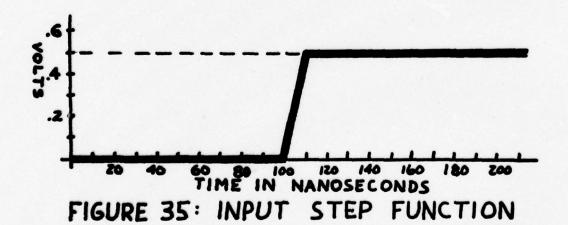
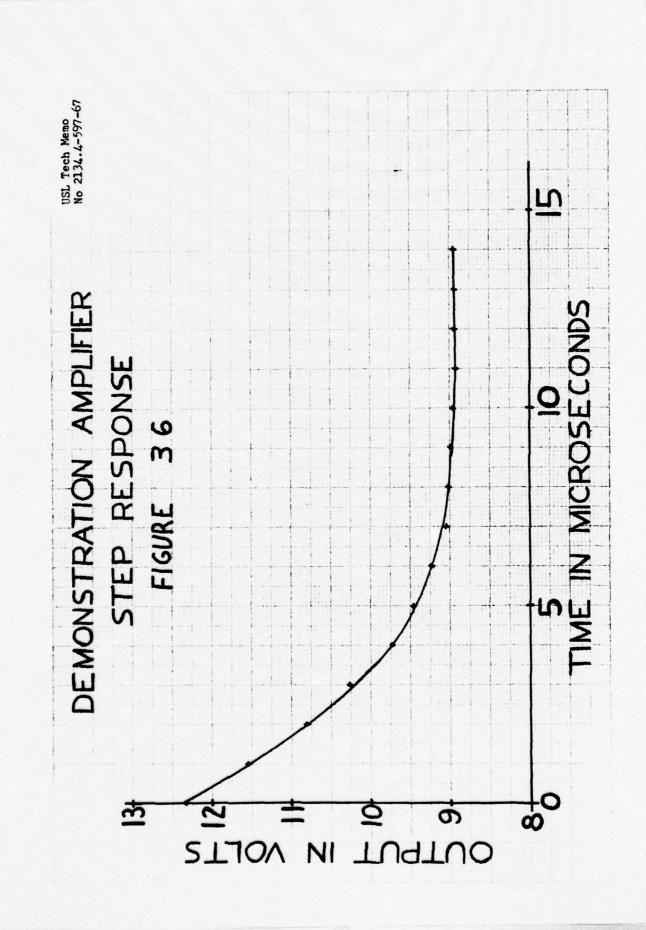


FIGURE 34: TRANSISTOR 2N 930 TRANSIENT MODELS





USL Tech Memo No 2134.4-597-67

# APPENDIX A

```
ECAP. IBM 704. A FILIPPINI. CODE 934.4. X 470
       DEMONSTRATION AMPLIFIER
0000
       PIAS ANALYSIS
       RUN 1. 30 JUNE 1966
       TRANSIENT ANALYSIS 0680
C
       THE CIPCUIT ELEMENTS
      N(1.0) .R=390E3
81
       N(4+1) +R=100F3
82
83
       N(4.0) .R=2.2F3
84
      N(2.0) .R=47E3
      N (5.3) .R=47E3
85
86
       N(0.5) .R=220
E6
       (1) .0 . 25
       G1 . 2N930
B9
       N(1.8) .R=1
810
       N(8+2) +R=(10E6+23+3E3)+E=-0+55
51
       B=10 • (10) • CFF
811
       N(8.2) .R=(10E6.5.25E3) .E==0.62
52
       B=11 . (11) . OFF
812
       N(8.2) .R=(10E6.3.74E3).E=-0.65
53
       B=12 . (12) . CFF
87
       N(6.2) .R=100
B13
       N(6.3) .R= (2E6.1)
      B=13 . (13) . OFF
54
B14
       N(3.6) .R=2E6
TI
       P(9+14) +BETA=200
C
       G2 . 2N930
B15
       N(3.9) .R=1
816
       N(9+4) +R=(10E6+23+3E3) +E=-0+55
35
       B=16 . (16) . OFF
817
       N(9+4) .R=(10E6.5.25E3) .E=-0.62
       B=17 . (17) .OFF
56
818
      N(9+4) +R=(10E6+3+74E3)+E==0+65
57
       E=18 . (18) . CFF
88
       N(7.4) .R=100
B19
       N(7.5) .R=(2E6.1)
       B=19.(19) .CFF
58
BZO
       N(5.7) .R=2E6
T2
       B(15.20) .BETA=200
       TIME STEP=1E-6
      FINAL TIME=1E-6
       PRINT. VCLTAGES
       EXECUTE
```

```
T = 0.
```

```
NCDES
                     VCLTAGES
                             -0.44727094E-00
  1-
          -0.15363346E-01
                                                 0.45212407E-00
                                                                   -0.24493132E-01
           0.45265925E-02
  5-
                             -0.44821733E-00
      8
                                                -0.25611684E-01
                                                                   -0.15363295E-01
  9-
      9
           C.45212413E-00
```

T = 0.2929687E-08

NCCES	VCLTAGE	5		
1- 4 5- 8 9- 9	-0.97963133E-02 0.77040417E-01 0.51959784E 00	-0.44292166E-00 -0.44385883E-00	0.51959780E 00 -0.18281265E-01	-0.17481074E-01 -0.97962618E-02

SWITCH 5 IS CN

 •	20	201		-	
 11.	/7	296	× /		() 6

NCDES		VCLTAG	ES		
1-	4	-C.15550889E-01	-0.44651127E-00	0.52468302E 00	-0.24756540E-01
5-	8	C.77786834E-01	-0.44745601E-00	-0.25886927E-01	-0.15550837E-01
9-	9	C.52468308E 00			

#### T = 0.3311443E-07

NODES		VCLTAGE	S		
1-		0.32121038E-00	-0.22741430E-00	0.97287805E 00	0.40073721E-00
5-	8	0.78861658E 00	-0.22789641E-00	0.41893829E-00	0.32121041E-00
9-	9	0-97287714F 00			

SWITCH 1 IS ON

#### T = 0.3311443E-07

NODES		VCLTAGE	ES		
1-	4	0.32167733E-00	-0.2282555E-00	0.97348746E 00	0.40131570E-00
5-	8	C.78856195E 00	-0.22873920E-00	0.41954306E-00	0.32167736E-00
9-	9	0.973486555 00			

## T = 0.1058197E-06

NODES	5	VCLTAGES	5		
1-	4	0.10229366E C1	0.47079632E-00	0.19096031E 01	0.12900408E 01
5-	8	C.25136025E C1	0.47179047E-00	0.13486478E 01	0.10229366E 01
9-	9	C.19096002E 01			

SWITCH 6 IS CN

#### T = 0.1058197E-06

NODES		VCLTA	GFS		
1-	4	U-10227955E 01	0.47065694E-00	0.19097744E 01	0.12898630E 01
5-	8	0.25136194E 01	0.47165079E-00	0.1348462ZE 01	0.10227965E 01
9-	9	0.190977155 01			

1 =	0.35119535-06					
NCCES 1- 4 5- 8 9- 9	VCLTAGES 0.34408688E 01 0.83287373E 01 0.50044745E 01 7 IS CN	0.28811011E 0.28871907E	).50044544E ).45522577E	PRO PE	0.43544181E 0.34408685E	01 01
T = NCDES 1- 4 5- 8 9- 9	C.3511953E-06  VCLTAGES C.34408967E 01 0.83287448E 01 0.50044554E 01	0.28811305E 0.28872201E	.50044553E .45522960E		0.43544535E 0.34408964E	01
T = NODES 1- 4 5- 8 9- 9	1.0000000E-06 VCLTAGES 0.98514202E 01 0.23702452E 02 0.13166107E 02	0.92714269E 0.92910255E	.13166136E .13045865E	_	0.12478881E 0.98514194E	

# APPENDIX B

```
FCAP. IFF 704. A FILIPPINI. CODE 934.4. X 470
C
C
      DENCMSTRATION AMPLIFIER
C
      TLK 1. 12 JLLY 1966
      DC ANALYSIS 0679
CC
      THE CIRCUIT ELEMENTS
81
      K(1.0) .R=390E3(.02)
62
      N(4.1) .R=100F3(.01)
      N (4.0) .R=2.2F3(.02)
83
      N(2.0) . R=47E3(.02)
84
25
      N(5+3) +R=47E3(.02)
86
      N(0.5) .R=220(.02) .E=25
      C1 . 2N930
C
      N(1+2) +R=23+3E3+E==0.55
89
87
      M (6.2) .R=100
B10
      N (3.6) .R=1E6
TI
      P(9+10) +BFTA=200
      G2 . 2N930
P11
      N(3+4) +R=2F3+E=-+63
      N(7.4) .R=100
88
B12
      N(5.7) .R=1F6
T2
      P(11.12) .PETA=200
C
      WCRST CASE . 1 . 2 . 3 . 4 . 5
      PRINT . CUPRENTS . BP
      EXECUTE
```

#### ELEMENT CURRENTS

BRANCHES	CLRRENTS			
1- 4	0.25239929E-04	0.26202131E-04	0.56653570E-02	0.19725858E-03
5- P	C.22456087E-03	0.588785196-02	0.19629239E-03	0.56632851E-02
9- 12	0.96219131E-06	0.19629779E-03	0.28262797E-04	0.56632339E-02

## ELEMENT POWER LOSSES

BRANCHES	PCWER LCS	SES		
1- 4	0.24845107E-03	0.68655168E-04	0.70611795E-01	0.18288145E-02
5- 6	0.23700966E-02	0.76266959E-02	-38530705E-05	0.32072799E-02
9- 12	0.21571422E-07	0.75761691E-03	0-15975714E-05	0.60452522E-01

#### WORST CASE SCLUTIONS FOR MODE VOLTAGES

NCDE	WCMIN	NCMINAL	WCMAX
1	C.96191663F C1	0.98435725F 01	0.10069151E 02
2	C.90468474F 01	0.92711534E 01	0.94966373E 01
3	C.12884086E C2	0-13150311E 02	0.13417452E 02
4	0.12197650F C2	0.12463785E 02	0.12730835E 02
5	C.23633743E C2	C.23704672E 02	C.237725CaF 02

T1 PETA=150 T2 PETA=150 EXECUTE

# ELEMENT CLARENTS

BRANCHES	CLERENTS			
1- 4	0.24767275E-04	0.26021074E=04	0.55733385E-02	0.19319198E=03
5- P	0.22894789E-03	0.57912912E=02	0.19193649E-03	0.55623434E=02
9- 12	0.12538192E-05	0.19193902E=03	0.37009779E-04	0.55623750E=02

# ELEMENT POWER LOSSES

BRANCHES	POWER LOS	SEE		
1- 4	0.23923299E-03	0.67709628E=04	0.68336625E-01	0.17541877E-02
5- 8	0.24636056E-02	0.73785920E=02	0.36839616E-05	0.30939665E-02
9- 12	0.36629057E-07	0.74206451E=03	0.27394474E-05	0.60676259E-01

# APPENDIX C

```
ECAP. IBM 704. A FILIPPINI. CODE 934.4. X 470
C
      CEMONSTRATION AMPLIFIER
C
C
      RLN 1. 13 JULY 1966
C
      AC ANALYSIS C678
C
C
      THE CIRCUIT ELEMENTS
      N(1.0) .R=390E3
81
82
      N(4+1) +R=100E3
83
      N (4.0) .R=2.2F3
      N (2+0) +R=47E3
84
85
      N (5+3) +R=47E3
86
      N(0.5) .R=220
P7
      N(0.6) .R=10E3.E=1
B8
      N(6+1) +C=1E-6
B9.
      N (4+1) +C=47E-12
810
      N(2.0) .C=4.7E-6
B11
      N (5+0) . C=60E-6
      G1 . 2N930
812
      N(1+7) +R=600
813
      N(7.2) .R=150
      N (3 . 7) .R=1E6
814
TI
      B(12.14) .BETA=170
B15
      1 (1.3) .C=9E-12
      G2. 2N930
816
      N (3.8) .R=600
817
      N(8.4) .R=6
818
      N (5+8) +R=1E6
12
      P(16.18) .RETA=220
B19
      N(3.5) .C=9E-12
      FREQUENCY=1E3
      PRINT . VOLTAGES
      EXECUTE
```

#### FREG = 0.99999999 03

# NCCES NODE VOLTAGES MAG 1- 4 0.35193714E-01 0.75729779E-02 0.95088840E 01 0.94705141F 01 -0.12766499E 02 -0.90298733E 02 0.17943960E 03 0.17943946E 03 MAG 5- 8 0.11080429E-01 0.41701452E-01 0.34395122E-01 0.94969132E 01 -0.89836828E 02 -0.33704266E 02 -0.13059527E 02 0.17943956E 03

MCDIFY
FREGUENCY=.1(2)57
EXECUTE

FREC = 0.99999999E-01

	NCDE	5	NODE VOLTAGES			
MAG PHA	1-	4	0.29921338F-01 0.84738354E 02	0.29823735E-01 0.84712443E 02	0.24034424F-01 -0.87310762F 02	0.24831239E-01 -0.87309933E 02
MAG	5-	8	0.24628855F-02 0.92006992E 02	0.99979306E 00 -0.35900725E-00	0.29918920F-01 0.84737742E 02	0.24902228E-01 -0.87310503F 02

FREC = 0.2000000F-00

	NCDE	5	NODE VI	OLTAGES		
MAG PHA	1-	4	0.59166153E-01 0.79552501F 02	0.58973136F-01 0.79500675F 02	0.50691719E-01 -0.84837802E 02	0.50482222E-01 -0.84836232E 02
MAG PHA	5-	8	0.49997230E-02 0.93819924F 02	C.99918994E 00 -0.71223165E 00	0.59161371F-01 0.79551274E 02	0.50626349E-01 -0.84837313E 02

FREG = 0.39999999E-00

	NCDE	5	NODE VO	CLTAGES	
MAG PHA	1-	4		0.11294783E-00 0.69573427E 02	
MAG PHA	5-	8		0.99701495F 00 -0.13828718E 01	

FREG = 0.79999999 00

NCDES		S	NODE VOLTAGES		
PAG PHA	1-	4		0.19575395E-00 0.52779137E 02	
PHA	5-	A		0.99088413F 00 -0.25343711E 01	

# FREG = 0.16000000F 01

	NCDE5		HOPE VOLTAGES				
MAG PHA	1-	4	0.27763262E-00 0.31637273E 02	0.27671977F-00 0.31222683E 02	0.56100322F 00 -0.82321507E 02	0.55872971F -0.82319245E	00
MAG PHA	5-	8	0.53746834F-01 0.59571081F 02	0.98070297E 00 -0.43592455E 01	0.27760985F-00 0.31627464E 02	0.56029382F -0.82320801E	00

# FREG = 0.31999999F 01

NCDES		5	NODE VI	nLTAGES			
MAG PHA	1-	4	0.31833018F-00 0.12085848F 02	0.31725867E-00 0.11256709E 02	0.13074625E 01 -0.90231179E 02	0.12025844E -0.90229888E	01 02
MAG PHA	5-	8		0.96919606E 00 -0.77386997E 01			

# FREG = 0.63999999F 01

NCCES		5	NODE VI	OLTAGES			
MAG PHA	1-	4	0.37245015E-00 -0.44886366F C1	0.32126407E-00 -0.61465853E 01	0.24303360E 0 -0.10060769E 0	1 0.24205264E 3 -0.10060703E	01 03
MAG Pha	5-	8		0.94485337E 00 -0.14613809E 02			

# FREG = 0.12799999E 02

	PICCE	S	NODE VOLTAGES			
MAG PHA	1-	4		0.29232989E-00 -0.24933373E 02		
MAG	5-	8		0.86420756F 00 -0.27384673F 02		

FREG = C.25549999F 02

	ACDES		NODE VOLTAGES		USL Tech Memo No 2134.4-597-67
PHA	1-	4	0.22422507F-00 0.22201126E-00 -0.39763315F 02 -0.46367864E 02	0.70230606F 01 -0.13607385F 03	0.69947210F 01 -0.13607369F 03
PHA	5-	A	0.28898535F-00 0.66606383F 00 -0.20789763F 02 -0.45435550E 02	0.22413822F=00 -0.39918631F 02	0.70142188F 01 -0.13607380F 03

FREG = 0.51199999E 02

NCDE		5	NODE V	VOLTAGES				
MAG	1-	4	0.13944293F-00 -0.52104613F 02	0.13540547E-00 -0.65142863E 02	0.86642677F 01 -0.15484248E 03	0.86293058F -0.15484241E	01	
MAG	5.	8	0.19190548F-00	0.41015550E-00 -0.61229800E 02	0.139245725-00	0 04533400=		

FREG = 0.10240000F 03

	NODES		NODE VOLTAGES				
MAG PHA	1-	4	0.79905955F-01 0.722707738 -0.52305789F 02 -0.771567468	E-01 E 02	0.92511273E 01 -0.16700297E 03	0.92436763E -0.16700295E	01
PHA	5-	8	0.10489667E-00 0.2213F733F -0.70263936E 02 -0.68569621E	E-00	0.7956R193E-01 -0.52R26516E 02	0.92694430E -0.16700296F	01

MCDIFY FREQUENCY=100(4)98F3 FXECUTE

FREG = 0.99999999 02

#### NCDES NOTE VOLTAGES

MAG 1\_ 4 0.81396223F=01 0.73921674E=01 0.92701083F 01 0.92327021E 01 -0.52513401E 02 -0.76850143E 02 -0.16669182F 03 -0.16669179E 03

MAG 5- 8 0.10724716E-00 0.22631206E-00 0.81045180E-01 0.92584382E 01
PHA -0.69792741F 02 -0.68473229E 02 -0.53026033F 02 -0.16669181E 03

FREG = 0.39999999 03

#### NCDES NODE VOLTAGES

MAG 1- 4 0.39229669E-01 0.18915925E-01 0.95000089E 01 0.94616748E 01 PHA -0.26213040E 02 -0.87281664E 02 -0.17734505E 03 -0.17734510E 03

MAG 5- 8 0.27665004E-01 0.67036746E-01 0.38515512E-01 0.94880492E 01 PHA -0.85600285F 02 -0.56080253E 02 -0.26799357F 02 -0.17734507E 03

FREG = 0.16000000E 04

#### NCDES NODE VOLTAGES

MAG 1- 4 0.34665667F-01 0.47297422E-02 0.95020253F 01 0.94636834F 01 PHA -0.96634780F 01 -0.91795272E 02 0.17776721F 03 0.17776698E 03

MAG 5- 8 0.69203722E-02 0.37633502E-01 0.33855870E-01 0.94900634E 01 PHA -0.91749703F 02 -0.24196494E 02 -0.98518427E 01 0.17776714E 03

FREG = 0.63999999F 04

#### MODE VOLTAGES

MAG 1- 4 0.33453641F-01 0.11581337E-02 0.93025136F 01 0.92649767F 01 PHΔ -0.12156725F 02 -0.10017825E 03 0.16802720F 03 0.16802626F 03

MAG 5- 8 0.1693x418F-02 0.34263654E-01 0.32653332F-01 0.92908027F 01 PHA -0.10166661F 03 -0.16084793E 02 -0.12205043E 02 0.16802691F 03

# FREG = 0.25600000F 05

	NCDES		NODE VOLTAGES				
MAG PHA	1-	4	0.26234575E-01 -0.34127139E 02	0.22583416E-03 -0.12362528E 03	0.72031499E 01 0.13922098E 03	0.71740842E 0.13921721E	
MAG PHA	5-	8	0.32793023F-03 -0.12996284E 03	0.26588344E-01 -0.35200594E 02	0.25610354E-01 -0.34132287E 02	0.71940818E 0.13921981E	01

# FREG = 0.10240000F 06

	NCDES		NODE VOLTAGES				
MAG PHA	1-	4		0.23024236E-04 -0.13726057E 03	0.26466995E 01 0.10606957E 03	0.26360209E 0.10605447E	
MAG PHA	5-	8	0.30162822E-04 -0.16077140E 03	0.10811292E-01 -0.47955360E 02	0.10443719E-01 -0.47387446E 02	0.26433679E 0.10606488E	

MCDIFY FREGUENCY=100E3(2)47F6 EXECUTE

## FREG = 0.9999999F 05

	NCDES		NODE VOLTAGES				
MAG PHA	1-	4			0.27051424E 01 0.10643865E 03		
MAG PHA	5-	8			0.10424544E-01 -0.47563134F 02	0.27017372F 0.10643407E	

# FREG = 0.20000000E 06

	NCDES		NODE VI	VOLTAGES			
MAG PHA	1-	4			0.13955137E 01 0.98261124E 02		
MAG PHA	5-	8	0.81746005E-05 -0.16559201E 03	0.71019799E-02 -0.37847707E 02	0.68887670E-02 -0.37315493E 02	0.13937577E 0.98251960E	

# FREG = 0.39999999 06

	NCDES		NODE V	OLTAGES			
MAG PHA	1-	4	0.55837984E-02 -0.23022410E 02	0.30787217E-05 -0.11296797E 03	0.70345215E 00 0.93886945E 02	0.70061835F 0.93827954E	00
MAG PHA	5-	8	0.20930562F-05 -0.16395189F 03	0.55994792E-02 -0.23394836E 02	0.54550592E-02 -0.23000559E 02	0.70256798E 0.93868619E	00

## FREQ = 0.79999999 06

	NCCES		NODE VOLTAGES			
PHA	1-	4	0.51419487E-02 -0.12534908F 02	0.14177517E-05 -0.10250553E 03	0.35245027E-00 0.91413754E 02	0.35103758F-00 0.91295779E 02
MAG PHA	5-	8	0.55587259F-06 -0.15517154E 03	0.51463030E-02 -0.12749983E 02	0.50241101F-02 -0.12521905F 02	0.35200936E-00 0.91377103E 02

## FREC = C.16COCCOCF 07

	NCDES		NOTE VOLTAGES			
MAG PHA	1-	4	0.50244781E-02 -0.68343458E 01	0.69271170E-06 -0.96819259E 02	0.17631731F-00 0.89641797E 02	0.17562484E-00 0.89405923E 02
MAG PHA	5•	8	0.16689225F-06 -0.13891519F 03	0.50256713E-02 -0.69463742E 01	0.49095478F-02 -0.68275206E 01	0.17610094E-00 0.89568517E 02

## FREG = 0.31999999F 07

	NCCES		NODE VOLTAGES			
MAG	1-	4	0.49934034F-02 -0.43378817F 01	0.34421779E-06 -0.94330221E 02	0.88173144F-01 0.87690546F 02	0.87855329E-01 0.87219385E 02
MAG PHA	5-	8	0.62240741E-07 -0.11986873F 03	0.49937820E-02 -0.43944973E 01	0.48792411E-02 -0.43344271E 01	0.88073329E-01 0.87544142F 02

#### FREG = 0.63999999F 07

	ACCES		NODE VOLTAGES			
MAG PHA	1-	4		0.17166847E-06 -0.93976703E 02		0.43992104E-01 0.83651243E 02
MAG PHA	5-	8	0.27871194F-07 -0.10516275F 03	0.49807840E-02 -0.46090102F 01	0.48667552F=02 -0.39788820F 01	0.44061081E-01 0.84297321F 02

## FREC = 0.12800000F 08

	+ CCES		NODE VOLTAGES			
PHA	1-	4	0.4957x579F-02 -0.55917761F 01	0.85438742E-07 -0.95589744E 02	0.22059800F-01 0.78819873E 02	0.22120820F-01 0.76980650F 02
MAG	5-	8			0.4944330gE-02 -0.5590g088F 01	

FREC = 0.25400000F 08

	NCDE	5	NODE V	OLTAGES		USL Tech Memo No 2134.4-597-67
MAG PHA	1-	4	0.48758C53F-02 -0.98530692F 01	0.42014069E-07 -0.99851977E 02	0.11054730E-01 0.67758239E 02	0.11298616E-01 0.64349214E 02
MAG PHA	5-	8	C.68382866F-08 -0.89215167E 02	0.48759119E-02 -0.98602310E 01	0.47643504E-02 +0.98526353E 01	0.11126426E-01 0.66680385E 02

# FREC = 0.51199999F 08

	NCDES		NODE VOLTAGES			
MAG PHA	1-	4		0.19775819E-07 -0.10804198E 03	0.55743287E-02 0.47662676E 02	0.60541371E-02 0.42508867E 02
MAG PHA	5-	8	0.36012533E-08 -0.83750853E 02	0.45901323E-02 -0.18046279E 02	0.44p51134E-02 -0.18042391E 02	0.57186734E-02 0.45964981E 02

# APPENDIX D

```
FCAP. IBM 704. A FILIPPINI. CODE 2134.4. X 470
C
      DEMONSTRATION AMPLIFIER
C
      RUN 1. 25 JANUARY 1967
C
      INITIAL VOLTAGES DERIVED FROM DC ANALYSIS OUTPUT DATA
C
      TRANSIENT ANALYSIS 0680
      THE CIRCUIT ELEMENTS
81
      N(1.0) .R=390E3
R2
      N(4+1) +R=100F3
83
      N(4.0) .R=2.2F3
B4
      N(2.0) .R=47E3
B5
      N(5.31 .R=47E3
B6
      N(0.5) .R=220.E=25
87
      N(0.6) .R=10E3
E7
      (1) .0.0.0.0.0.0.0.0.0.0.0.0.0.5E-1
      N(6+1) +C=1E-6+E0=9.8514202
88
89
      N(4.1) .C=47E-12.E0=-2.6274608
B10
      N(2.0) .C=4.7E-6.E0=-9.2714269
      Q1 . 2N930
811
      N(1.7) .R=2E3
812
      N(7.2) .R=(22.4E3.10E6) .E=-0.55
51
      B=12 . (12) .ON
B13
      N(7+2) +R=(10E6+2.54E3) +E=-0.614
52
      R=13 . (13) .OFF
P14
      N(7.2) .R=(10F6.1) .E=-0.63
53
      B=14 . (14) . OFF
815
      N(8+21+R=100
      N(8+3) +R= (2E6+1)
B16
54
      R=16 . (16) .OFF
817
      N(3.8) .R=2F6
TI
      A(11+17) +BETA=220
A18
      N(1+3) +C=9E-12+E0=3.3147158
      Q2 . 2N930
B19
      N(3.9) .R=2E3
      N(9+4) +R=(22.4E3+10E6) +E==0.55
P20
55
      P=20 . (20) .ON
821
      N(9+4) +R=(2.54E3+10E6) +E==0.614
56
      A=21 . (21) .CN
P22
      N(9+4) +R=(1+10E6) +E=-0+63
57
      A=22 . (22) .ON
B23
      N(10+4) .R=100
B24
      N(10.5) .Q=(2E6.1)
58
      R=24 . (24) .OFF
B25
      N15-101 .R=2E6
TZ
      B(19.25) .BETA=170
826
      N(3.5) .C=9E-12.E0=10.5363160
      TIME STEP = 10E-9
      OUTPUT INTERVAL = 100
      FINAL TIME = 20E-6
      PRINT. VOLTAGES
      FXECUTE
```

NODEC	VOLTAGES		USL Tech Memo No 2134.4-597-67
NODES	VOLTAGES 0.98462394E 01 0.92714269E 01 0.13160963E	02	0.12473693E 02
1- 4	0.23697288E 02 -0.51800013E=02 0.98442239E	-	0.92939842E 01
9- 10	0.13103711E 02 0.12961409E 02		
T s	0.999996F=06		
NODES	VOLTAGES	- 0-	0 114053305 03
1- 4	0.98464921E 01		0.11695328E 02 0.92941272E 01
5- A 9- 10	0.12325349E 02 0.12221736E 02	. •1	- + + + + + + + + + + + + + + + + + + +
T .	0.1999999F-05		
NODES	VOLTAGES 0 027142485 01 0 114594455	. 02	0.10970663E 02
1- 4 5- A	0.98482691E 01		0.92956724E 01
9- 10	0.11600682E 02 0.11464603E 02		
T =	0.2999997E-05		
NODES	VOLTAGES		
NUUES	0.98494508E 01 0.92714275E 01 0.11105766E	02	0.10420665E 02
5- R	0.23906120E 02 -0.18819571E-02 0.98471709E		0.92966845E 01
9- 10	0.11050683E 02 0.10890192E 02		
1 .	0.399994E-05		
NODES	VOLTAGES		
1- 4	0.98508728E 01 0.92714275E 01 0.10631614E		0.99490780E 01
5- A	0.23951691E 02 -0.42974949E-03 0.984847598		0.92979258E 01
9- 10	0.10579094E 02 0.10396821E 02		
7.	0.4999989E-05		
NODES	VOLTAGES		
NUDES 4	0.98513377E 01 0.92714275E 01 0.10300975	E 02	0.96201170E 01
5- A	0.2399178FE 02 0.78082085E-04 0.984890251		0.92983145E 01
9- 10	0.10250133E 02 0.10053636E 02		
7.	0.5999984E-05		
NODES	VOLTAGES		
1- 4	0.98521334E 01 0.92714275E 01 0.10036411	E C2	0.93569901E 01
5- A	0.24C07225E 02 0.92089176E-03 0.98496326		0.92990089E 01
9- 10	0.99870047E 01 0.97783557E 01		*

				USL Tech Memo No 2134.4-597-67
T =	0.6999979F-05			NO 2234.4-377-4.
NODES	VOLTAGES			
1- 4 5- 8	0.98522616E 01 0.24023513E 02	0.92714275E 01 0.10905266E-02	0.98476982E 01 0.98497504E 01	0.91691850E 01 0.92991079E 01
9- 10	0.97991993E 01	0.95828641E 01	0.,044,0045 (1	0.727710176 01
T s	0.7999972E=05			
NODES	VOLTAGES			
1- 4	0.98529601E 01	0.92714275F 01	0.98207664E C1	0.91425133E 01
5- A 9- 10	0.24027519E 02 0.97725275E 01	0.18339157E=02 0.95540047E 01	0.98503914E 01	0.92997351E 01
,		34,22,4004,12 01		
T =	0.8999962F=05			
NODES	VOLTAGES 0.98529541E 01	0.92714275F 01	0.98208122E 01	0.91425570E 01
5- 8	0.24027542E 02	0.19726587E-02	0.98503858E Q1	0.92997321E 01
9- 10	0.97725712E 01	0.95540506E 01		
T =	0.9999951F=05			
NODES	VOLTAGES			
1- 4	0.98517643E 01	0.92714275E 01	0.98219490E 01	0.91434628E 01
5- 8 9- 10	0.24024597E 02 0.97734770E 01	0.72705746E-03 0.95569271E 01	0.98492941E 01	0.92986539E 01
<b>3-</b> 10	0.777347702 01	0.499048115 01		
T .	0.1099994E=04			
NODES	VOLTAGES			
1- 4	0.98518203E 01	0.92714275E 01	0.98263016E 01	0,91477937E 01
5- 8	0.24024101E 02	0.82802773E-03	0.98493453E 01	0.92987059E 01
9- 10	0.97778079E 01	0.95614742E 01		
TE	0.1199993F=04			
NODES	VOI TACES			
NODES	VOLTAGES 0.98517635E 01	0.92714275E 01	0.98220482E 01	0.91435602E 01
5- A	0.2402452HE 02	0.81598759E-03	0.98492933E 01	0.92986543F 01
9- 10	0.97735743E 01	0.955702896 01		
T =	0.1299992F=04			
NODES	VOLTAGES 0.98524883E 01	0.92714275E 01	0.97993889E 01	0.91211402E 01
5- A	0.24028061E UZ	0.15865564E-02	0.98499584E 01	0.979930936 01
9- 10	0.97511544E 01	0.95326164E 01		

		USL Tech Memo No 2134.4-597-67
T =	0.1399991F=04	
NODES 1- 4 5- 8 9- 10	VOLTAGES 0.98518893E 01	0.91057754E 01 0.92987610E 01
T =	0.1499990F=04	
NODES	VOLTAGES	
1- 4 5- 8 9- 10	0.98531505E 01	0.90775874E 01 0.92999011E 01
T .	0.1599989F+04	
NODES 1- 4 5- 8 9- 10	VOLTAGES 0.98527297E 01	0,90349531E 01 0,92995153E 01
T .	0.1699988E-04	
NODES 1- 4 5- 8 9- 10	VOLTAGES 0.98528096E 01	0.90076334E 01 0.92995859E 01
T .	0.1799987E-04	
NODES 1- 4 5- 8 9- 10	VOLTAGES 0.98533887E 01  0.92714275E 01  0.96773224E 01 0.24041221E 02  0.27261972E=02  0.98507846E 01 0.96298661E 01  0.94047540E 01	0.89998522E 01 0.93001106E 01
Т.	0.1899986E-04	
NODES 1- 4 5- 8 9- 10	VOLTAGES  0.98528350E 01	0.89993218E 01 0.92996089E 01
T .	0.19999R5F-04	
NODES 1- 4 5- 8	0.98522653E 01	0.90029976E 01 0.92990921E 01

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9- 10 0.96330115E 01 0.94099881E 01

T = 0.2000984E-04

NODE	5	VOLTAGE	5		
1-	4	0.98528981E 01	0.92714275F 01	0.96812820E 01	0.90036649E 01
5-	R	0.24039169E 02	0.23356676E-02	0.98503346E 01	0.92996643E 01
9-	10	0.96336788E 01	0.94097313E 01		

#### APPENDIX E

#### Outline of this Memorandum

#### I INTRODUCTION

- A. Contents of Memo
- B. Purpose of Memo

#### II SECTION I: PROGRAM DESCRIPTION

- A. Purpose of ECAP
- B. Three Programs in One
  - 1. DC Analysis Program
  - 2. AC Analysis Program
  - 3. Transient Analysis Program
- C. Usefullness of ECAP

#### III SECTION II: PROGRAMMING SOFTWARE

- A. Two Forms are used
  - 1. Production Request
  - 2. Fortran Coding Form
- B. Punch Cards Used
  - 1. Time Cards
  - 2. Comment Cards
    - a. Line Spaces, etc.
    - b. Identification Cards
  - 3. Command Cards
    - a. AC Analysis Card
    - b. DC Analysis Card
    - c. Transient Analysis Card
    - d. Execute Card
    - e. Modify Card
  - 4. Data Cards
    - a. The Standard Brach
    - b. B-Cards
    - c. T-Cards
    - d. M-Cards
    - e. S-Cards
    - f. Source Cards
      - (1) Non-Periodic
      - (2) Periodic
      - (3) Sinusoidal

- g. Use of Data Cards
- h. Continuation Cards
- i. Limitations on Data Cards
- j. Maximum: 50 Nodes
- k. Modified Data Cards
- 5. Solution Control Cards
  - a. For AC Analysis
    - (1) Frequency Card
    - (2) Modified Frequency Card
  - b. For DC Analysis
    - (1) Sansitivity Card (2) Worst Case Card

    - (3) Standard Deviation Card
  - c. For Transient Analysis
    - (1) Time Step Card
    - (2) Output Interval Card
    - (3) Initial Time Card
    - (4) Final Time Card
    - (5) Equilibrium Card

    - (6) Short Card (7) Open Card (8) 1 Error Card

    - (9) 2 Error Card
    - (10) 3 Error Card
- 6. Output Specification Cards
  - a. For AC and DC Analysis
  - - (1) Print Node Voltages
    - (2) Print Element Voltages
    - (3) Print Branch Voltages
    - (4) Print Element Currents
    - (5) Print Branch Currents
    - (6) Print Element Power Dissipations
    - (7) Print Miscellaneous Outputs
  - b. For Transient Analysis
    - (1) Print Node Voltages
    - (2) Print Element Currents

# SECTION III: COMPUTING PROCEDURE

- A. Recommended Procedure
- B. Demonstrate Procedure
  - 1. DC Bias Point Analysis
    - a. Draw DC Diagram
    - b. Model Non-Linear Devices
    - c. Document ECAP Data
    - d. Assist Computer Center Personnel

- (1) Have Cards Punched
- (2) Assemble Card Deck
- (3) Fill in Production Log (4) Submit Data Cards (5) Retrieve Output Data

- 2. DC Worst Case Analysis
- 3. AC Analysis (Frequency Response)
  4. Transient Analysis (Step Response)

#### V SUMMARY

- A. Restate Purpose of Memo
- B. Restate Purpose of ECAP
- VI REFERENCES
- VII FIGURES
- VIII APPENDICES